

WHAT IS CLAIMED IS:

- 1 1. A method of selecting decoupling capacitors for a packaged semiconductor chip,  
2 comprising:  
3 grouping at least some chip leads on the packaged semiconductor chip into at least two  
4 regions;  
5 for each of the regions, determining a first lead count for the chip leads in a first lead  
6 category in that region;  
7 for each of the regions, determining a second lead count for the chip leads in a second  
8 lead category, if any, in that region;  
9 for each of the regions, determining a third lead count for the chip leads in a third lead  
10 category, if any, in that region;  
11 for each lead category in each of the regions, determining a total switching current for  
12 that lead category in that region based on the lead count for that lead category in that region;  
13 for each lead category in each of the regions, determining a total decoupling capacitance  
14 value for that lead category in that region based on the total switching current for that lead  
15 category in that region, a maximum allowable voltage ripple selected for that lead category, and  
16 a voltage rise time selected for that lead category;  
17 determining how many decoupling capacitors may be allocated to each of the regions;  
18 for each of the regions, allocating a number of the decoupling capacitors for that region to  
19 each lead category;  
20 for each lead category in each of the regions, dividing the total decoupling capacitance  
21 value for that lead category in that region by the number of the decoupling capacitors allocated  
22 for that lead category in that region to obtain a desired individual capacitance value for each of

23 the decoupling capacitors allocated for that lead category in that region; and  
24 for each lead category in each of the regions, selecting an actual decoupling capacitor for  
25 each of the decoupling capacitors allocated for that lead category in that region, wherein each of  
26 the actual decoupling capacitors has an actual individual capacitance corresponding to the  
27 desired individual capacitance value for that allocated decoupling capacitor of that lead category  
28 in that region, and wherein each of the actual decoupling capacitors of that lead category has a  
29 self-resonance frequency selected based on an operating frequency of the chip leads in that lead  
30 category.

1 2. The method of claim 1, further comprising:

2 selecting at least one bulk capacitor for at least one of the regions.

1 3. The method of claim 1, further comprising:

2 for at least one of the regions, selecting a bulk capacitor having a bulk capacitance of  
3 about or greater than ten times the total decoupling capacitance value for that region.

1 4. The method of claim 1, wherein the first lead category comprises core supply voltage  
2 leads.

1 5. The method of claim 4, wherein the second lead category comprises a first group of  
2 input/output supply voltage leads.

1 6. The method of claim 5, wherein the third lead category comprises a second group of  
2 input/output supply voltage leads, and wherein the third lead category has a different operating  
3 frequency than the second lead category.

- 1 7. The method of claim 1, wherein each of the lead categories has a different operating  
2 frequency.
- 1 8. The method of claim 1, wherein at least some of the lead categories have different supply  
2 voltage levels.
- 1 9. The method of claim 1, wherein at least some of the lead categories have different  
2 switching current levels.
- 1 10. The method of claim 1, wherein the total switching current is a total peak switching  
2 current.
- 1 11. The method of claim 1, wherein the selected voltage rise time for each lead category is an  
2 estimated voltage rise time based on specifications for the packaged semiconductor chip.
- 1 12. The method of claim 1, wherein the selected maximum allowable voltage ripple for each  
2 lead category is an estimated maximum allowable voltage ripple based on specifications for the  
3 packaged semiconductor chip.
- 1 13. The method of claim 1, wherein the selected self-resonance frequency for the actual  
2 decoupling capacitors is about the same as the operating frequency of the chip leads in that lead  
3 category.
- 1 14. The method of claim 1, wherein the grouping of chip leads yields a number of regions  
2 selected from a group consisting of two, three, four, five, six, seven, eight, nine, and ten.

1 15. The method of claim 1, wherein the actual individual capacitance is about equal to or  
2 greater than the desired individual capacitance value for that allocated decoupling capacitor of  
3 that lead category in that region.

1 16. The method of claim 1, wherein the grouping of chip leads into regions is based upon  
2 considering switching frequencies of the leads.

1 17. A method of manufacturing an electronic device comprising the method of claim 1.

1 18. A method of assembling a computer system comprising the method of claim 1.

1 19. A method of selecting decoupling capacitors for a packaged semiconductor chip,  
2 comprising:  
3       grouping at least some chip leads on the packaged semiconductor chip into at least two  
4 regions;  
5       determining a first lead count for the chip leads in a first lead category in a selected  
6 region;  
7       determining a second lead count for the chip leads in a second lead category, if any, in  
8 the selected region;  
9       for each lead category in the selected region, determining a total switching current for  
10 that lead category in the selected region based on the lead count for that lead category in the  
11 selected region;  
12       for each lead category in the selected region, determining a total decoupling capacitance  
13 value for that lead category in the selected region based on the total switching current for that  
14 lead category in the selected region;  
15       allocating a number of decoupling capacitors to each lead category of the selected region;  
16       for each lead category in the selected region, dividing the total decoupling capacitance  
17 value for that lead category by the number of the decoupling capacitors allocated for that lead  
18 category in the selected region to obtain a desired individual capacitance value for each of the  
19 decoupling capacitors allocated for that lead category in the selected region; and  
20       for each lead category in the selected region, selecting an actual decoupling capacitor for  
21 each of the decoupling capacitors allocated for that lead category, wherein each of the actual  
22 decoupling capacitors has an actual individual capacitance corresponding to the desired

23 individual capacitance value for that allocated decoupling capacitor of that lead category in the  
24 selected region.

1 20. A method of manufacturing an electronic device comprising the method of claim 19.

1 21. A method of assembling a computer system comprising the method of claim 19.

1 22. An electronic device comprising:

2 a packaged semiconductor chip having a plurality of chip leads extending therefrom,

3 a first group of the decoupling capacitors electrically connected to a first select group of  
4 the chip leads in a first select region of the chip leads, the first group of decoupling capacitors  
5 each having a first decoupling capacitance and each having a first self-resonance frequency;

6 a second group of the decoupling capacitors electrically connected to a second select  
7 group of the chip leads in the first select region of the chip leads, the second group of decoupling  
8 capacitors each having a second decoupling capacitance and each having a second self-resonance  
9 frequency, wherein the second decoupling capacitance differs from the first decoupling  
10 capacitance, and wherein the second self-resonance frequency differs from the first self-  
11 resonance frequency; and

12 a first bulk capacitor electrically connected to at least one of the first select group of the  
13 chip leads in the first select region, the first bulk capacitor having a first bulk capacitance,  
14 wherein the first bulk capacitance differs from the first and second decoupling capacitances.

1 23. The electronic device of claim 22, further comprising:

2 a third group of the decoupling capacitors electrically connected to a third select group of  
3 the chip leads in a second select region of the chip leads, the third group of decoupling capacitors  
4 each having a third decoupling capacitance and each having a third self-resonance frequency;

5 a fourth group of the decoupling capacitors electrically connected to a fourth select group  
6 of the chip leads in the second select region of the chip leads, the fourth group of decoupling  
7 capacitors each having a fourth decoupling capacitance and each having a fourth self-resonance  
8 frequency, wherein the fourth decoupling capacitance differs from the third decoupling  
9 capacitance, and wherein the fourth self-resonance frequency differs from the third self-

10 resonance frequency; and

11 a second bulk capacitor electrically connected to at least one of the third select group of  
12 the chip leads in the second select region, the second bulk capacitor having a second bulk  
13 capacitance, wherein the second bulk capacitance differs from the third and fourth decoupling  
14 capacitances.

1 24. The electronic device of claim 23, wherein the third decoupling capacitance is about the  
2 same as the first decoupling capacitance, and wherein the second bulk capacitance is about the  
3 same as the first bulk capacitance.

1 25. The electronic device of claim 22, wherein the first and second groups of the decoupling  
2 capacitors are located within the packaged semiconductor chip.

1 26. The electronic device of claim 22, further comprising:  
2 a circuit board electrically connected to the packaged semiconductor chip, wherein the  
3 first and second groups of the decoupling capacitors are located on the circuit board.

1 27. The electronic device of claim 22, further comprising:  
2 a circuit board electrically connected to the packaged semiconductor chip, wherein the  
3 first and second groups of the decoupling capacitors are located at least partially within the  
4 circuit board.